Yaotian Liu

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Education

Arizona State University 2023/08 – 2028/06 (Expected)
PhD in Computer Engineering Tempe, Arizona, US
- GPA: 4.0/4.0

Shanghai Jiao Tong University 2019/09 – 2023/06
Bachelor of Engineering in Microelectronics Science and Engineering Shanghai, China
- GPA: 3.7/4.3. Rank 19/67.
- Outstanding Graduates

Work Experience

Shanghai Taize Semiconductor 2022/06 – 2022/09, 2023/03 – 2023/06
Digital IC Design Intern Shanghai, China
- Developed the micro-architecture for the data link layer of the company's proprietary inter-chip connection, supporting 1024 chips. Co-author of a related patent. The design has been successfully taped out using TSMC 16 nm.
- Developed an accelerator for elliptic curve accumulation in Elliptic Curve Cryptography (ECC).

Research Experience

Arizona State University, ECEE 2023/08 – Now
Research Assistant, advised by Prof. Jeff Zhang Tempe, AZ, US
- **Skip-SCAR: Hardware-Friendly High-Quality Embodied Visual Navigation**
  - The first computation-efficient ObjectNav system features a skip mechanism and a novel SCAR-based predictor that leverage sparsity to significantly reduce memory usage.
  - Currently No.1 among all published methods in the online leaderboard.
- **Intel 16nm Tapeout**
  - Designed, implemented and verified a systolic array with AXI interfaces in SystemC and Catapult HLS.
  - Designed, implemented and verified a RISC-V & AXI based SoC design in SystemVerilog, which supports arbitrary number of accerlerators and memories.
  - Developed an agile physical design flow using Synopsys Fusion Compiler, PrimeTime.
  - Setup multiple automatic scripts to speed up relative flows.
    - A flow to transfer memory IPs from SystemVerilog to Verilog and then generate a Catapult memory library by automatically extracting relevant information from the Verilog code and datasheet.
    - An automatic Docker-based RISC-V cross-compilation flow, able to run on any type of host machine.
    - A flow to run CVA6 (a RISC-V code) simulation with Verilator to generate waveform.
- **LLM-VeriPPA**
  - Developed a Python workflow to automatically extract information from Verilog code, perform logic synthesis for PPA (Power, Performance, and Area), and iteratively reduce the clock period to find the fastest possible timing.

Shanghai Jiao Tong University, Department of Micro/Nano Electronics 2023/01 – 2023/05
Final Year Project, advised by Prof. Yongfu Li Shanghai, China
- Implemented a functional ECO system with a Verilg parser written in PEG grammar, accepted by AICAS 2023.
- An ABC-based algorithm for efficient circuit pruning by removing functionally equivalent sub-circuits, which increase the performance of functional ECO.

Shanghai Jiao Tong University, AI Institute 2022/05 – 2022/09
Undergraduate Research Assistant, advised by Prof. Yunbo Wang Shanghai, China
- Implemented a reinforcement learning algorithm for automatically stock trading.
- Reproduced an baseline algorithm ytliu/FactorVAE (60+ stars) from AAAI 2022.

Publications

- Liu, Y., Cao, Y., Zhang, J., "Skip-SCAR: Hardware-Friendly High-Quality Embodied Visual Navigation." *arXiv preprint arXiv: 2405.14154*.

Update time: 2025-05-01

- Nalla, P., Haque, E., Liu, Y., Sapatnekar S., Zhang, J., Chakrabarti, C., Cao, Y., "CLAIRE: Composable Chiplet Libraries for AI Inference" *2025 Design Automation and Test in Europe Conference (DATE)*
- Wang, Z., Sun, J., Goksoy, A., Mandal, S., Liu, Y., Seo, J., etc. "Exploiting 2.5D/3D Heterogeneous Integration for AI Computing," *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC)*
- Thorat, K., Zhao, J., Liu, Y., Peng, H., Xie, X., Lei, B., Zhang, J. and Ding, C.. "Advanced Language Model-Driven Verilog Development: Enhancing Power, Performance, and Area Optimization in Code Synthesis." *arXiv preprint arXiv:2312.01022.*
- Liu, Y., Zhang, Y., Zhang, Q., Chen, R. and Li, Y., 2023, June. "FEEP: Functional ECO synthesis with efficient patch minimization." In 2023 *IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS).*

Open-Sourse Project

obsidian-pseudocode ytliu74/obsidian-pseudocode (100+ stars)
- An Obsidian plugin that renders LaTeX-style pseudocode in a code block, offering various auxiliary features.

simple SPICE ytliu74/SimpleEDA (7 stars)
- A basic SPICE tool for circuit simulation supports DC, AC, and TRAN analysis for linear and nonlinear devices with a GTK interface.

Skills

Programming Languages: Verilog, Python, C/C++, Javascript/Typescript.
Tech Skills: Git, Digital Logic Design, Pytorch, Linux, Docker, Matlab, RTL to GDSII flow...

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